

## ABSTRACT

A data interpolating device comprises plural stages of delay circuits (1-1, 2-1, 3-1) for delaying discrete data sequentially inputted and multiplication/addition circuits (4-1 to 16-1) that performs weighted addition of data outputted from the output stages of the plural stages of delay circuits (1-1, 2-1, 3-1) according to the value of a digital basic function (-1, 1, 8, 8, 1, -1) and thereby determine interpolation data. Since a sampling function of finite supports differentiable once or more times over the whole range.